Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

****

**PAD FUNCTIONS:**

1. **NC**
2. **-VS**
3. **-VS**
4. **-VS**
5. **-VS**
6. **NC**
7. **-IN**
8. **+IN**
9. **NC**
10. **NC**
11. **NC**
12. **CURRENT SENSE**
13. **+VS**
14. **+VS**
15. **+VS**
16. **+VS**
17. **CURRENT SENSE**
18. **OUTPUT DRIVE**
19. **OUTPUT DRIVE**
20. **OUTPUT DRIVE**
21. **OUTPUT DRIVE**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: -Vs**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .214” X .205” DATE: 9/28/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .000” P/N: OPA541SD**

**DG 10.1.2**

#### Rev B, 7/19/02